WHAT IS CLAIMED IS:

1. A method of providing emulation information indicative of internal operations of a data processor for use by an apparatus external to the data processor, comprising:

providing a stream of emulation trace information indicative of data processing operations performed by the data processor;

providing a stream of timing information indicative of operation of a clock used by the data processor to perform data processing operations; and

inserting in the trace stream and in the timing stream information indicative of a temporal relationship between the trace information and the timing information.

2. The method of Claim 1, wherein said step of providing a timing stream includes providing a plurality of bits which are respectively indicative of a plurality of cycles of said clock.

3. The method of Claim 2, wherein said inserting step includes inserting mutually corresponding identifiers in both the trace stream and the timing stream, and inserting in one of the streams an index for identifying a bit of the timing stream which represents a clock cycle that timewise corresponds to data in the trace stream at a point in the trace stream at which the trace stream identifier is inserted.

4. The method of Claim 3, wherein said index inserting step includes inserting said index into the trace stream.

5. The method of Claim 4, wherein said trace information includes program counter values associated with said data processing operations.

6. The method of Claim 3, wherein said bit providing step includes arranging groups of said bits into respective packets within the timing stream, said identifier inserting step including inserting one of said identifiers into the timing stream at a predetermined position relative to one of said packets.

7. The method of Claim 6, wherein said one packet includes the bit identified by said index.

8. The method of Claim 7, wherein said index inserting step includes inserting said index into the trace stream.

9. The method of Claim 7, wherein said index identifies a bit position within said one packet occupied by the identified bit.

10. The method of Claim 9, wherein said index inserting step includes inserting said index into the trace stream.

11. The method of Claim 3, including providing a further stream of emulation trace information indicative of data processing operations performed by the data processor, and inserting into the further trace stream an identifier which corresponds to said mutually corresponding identifiers.

12. The method of Claim 11, wherein one of said trace streams includes program counter values associated with said data processing operations.

13. The method of Claim 12, wherein the other trace stream includes memory reference information indicative of a memory access associated with said data processing operations.

14. The method of Claim 11, wherein one of said trace streams includes memory reference information indicative of a memory access associated with said data processing operations.

15. The method of Claim 11, including combining the trace streams and the timing stream into a single composite stream.

16. The method of Claim 1, wherein said trace information includes memory reference information indicative of a memory access associated with said data processing operations.

17. The method of Claim 1, wherein said trace information includes program counter values associated with said data processing operations.

18. The method of Claim 1, including combining the trace stream and the timing stream into a single composite stream.

19. An apparatus for providing emulation information indicative of internal operations of a data processor for use by an apparatus external to the data processor, comprising:

a first input for coupling to the data processor;

a trace generator coupled to said first input for providing a stream of emulation trace information indicative of data processing operations performed by the data processor;

a second input for coupling to the data processor;

a timing generator coupled to said second input for providing a stream of timing information indicative of operation of a clock used by the data processor to perform data processing operations; and

said trace generator and said timing generator cooperable for inserting into the trace stream and the timing stream information indicative of a temporal relationship between the trace information and the timing information.

20. The apparatus of Claim 19, wherein said timing generator is operable for providing in said timing stream a plurality of bits which are respectively indicative of a plurality of cycles of said clock.

21. The apparatus of Claim 20, wherein said trace generator and said timing generator are cooperable for inserting mutually corresponding identifiers into the trace stream and the timing stream, respectively, one of said trace and timing generators further operable for inserting in its associated stream an index for identifying a bit of the timing

stream which represents a clock cycle that timewise corresponds to data in the trace stream at a point in the trace stream at which the trace stream identifier is inserted.

22. The apparatus of Claim 21, wherein said timing generator is operable for arranging groups of said bits into respective packets within the timing stream and for inserting its associated identifier into the timing stream at a predetermined position relative to one of said packets.

23. The apparatus of Claim 22, wherein said one packet includes the bit identified by said index.

24. The apparatus of Claim 21, wherein said one generator is said trace generator.

25. The apparatus of Claim 19, including a combiner coupled to said trace generator and said timing generator for combining said trace stream and said timing stream into a composite stream.

26. An integrated circuit, comprising:

a data processor for performing data processing operations;

an apparatus coupled to said data processor for providing emulation information indicative of said data processing operations to an emulation apparatus located externally of said integrated circuit, including a trace generator for providing a stream of emulation trace information indicative of said data processing operations, and a

timing generator for providing a stream of timing information indicative of operation of a clock used by said data processor to perform said data processing operations; and

said trace generator and said timing generator cooperable for inserting into the trace stream and the timing stream information indicative of a temporal relationship between the trace information and the timing information.

27. A data processing system, comprising:

an integrated circuit including a data processor for performing data processing operations;

an emulation controller located externally of said integrated circuit and coupled thereto for controlling emulation operations of said data processor;

said integrated circuit including an apparatus coupled between said data processor and said emulation controller for providing to said emulation controller emulation information indicative of said data processing operations, said apparatus including a trace generator for providing a stream of emulation trace information indicative of said data processing operations, and a timing generator for providing a stream of timing information indicative of operation of a clock used by said data processor to perform said data processing operations; and

said trace generator and said timing generator cooperable for inserting into the trace stream and the timing stream information indicative of a temporal relationship between the trace information and the timing information.

28. The system of Claim 27, including a man/machine interface coupled to said emulation controller for permitting a user to communicate with said emulation controller.

29. The system of Claim 28, wherein said man/machine interface includes one of a visual interface and a tactile interface.